TVS3V3L4U

Protection device

TVS (transient voltage suppressor)
Bi/uni-directional, 3.3 V, 2 pF, RoHS and halogen free compliant

Feature list

- ESD/Transient/Surge protection according to:
  - IEC61000-4-2 (ESD): ±30 kV (air/contact discharge)
  - IEC61000-4-4 (EFT): ±4 kV/±80 A (5/50 ns)
  - IEC61000-4-5 (Surge): ±20 A (8/20 µs)
- Reverse working voltage up to: V_{RWM} = 3.3 V
- Low leakage current: I_R <50 nA
- Low capacitance: C_L = 2 pF (typical, I/O to GND), 1 pF (typical, I/O to I/O)
- Low clamping voltage: V_{CL} = 7.7 V (typical) at I_{pp} = 20 A (8/20 µs)
- Pb-free (RoHS compliant) and halogen free package

Potential applications

- 10/100/1000 Ethernet
- 4 lines uni-directional (pin 1, 3, 4, 6 to GND)
- 2 lines bi-directional (pin 2 n.c.)

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

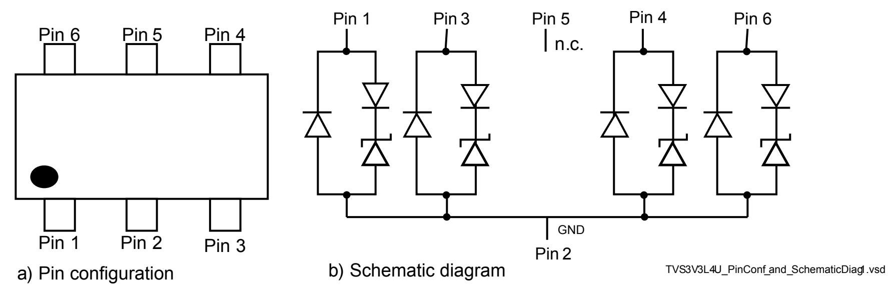

Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
TVS3V3L4U	SC74-6-2	4-lines uni-directional or 2-lines bi-directional	E1s

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1 Maximum ratings

Note: *T_A = 25 °C, unless otherwise specified.*

Table 2 Maximum ratings

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
ESD discharge [1]	V_{ESD}	-30	30	kV	air
		-30	30		contact
Peak pulse current	I_{pp}	-20	20	A	t_p = 8/20 µs [2]
Peak pulse power	P_{PK}	–	154	W	t_p = 8/20 µs [2]
		–	1044		t_p = 100 ns [3]
Operating temperature	T_{OP}	-55	125	°C	–
Storage temperature	T_{stg}	-55	150		–

Attention: ***Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.***

1 V_{ESD} according to IEC61000-4-2
2 I_{pp} according to IEC61000-4-5. $P_{PK}$is calculated by I_{pp} x V_{CL}
3 Please refer to AN210 [1]. P_{PK} is calculated by I_{TLP} x V_{CL}

2 Electrical characteristics

Note: *T_A = 25 °C, unless otherwise specified.*

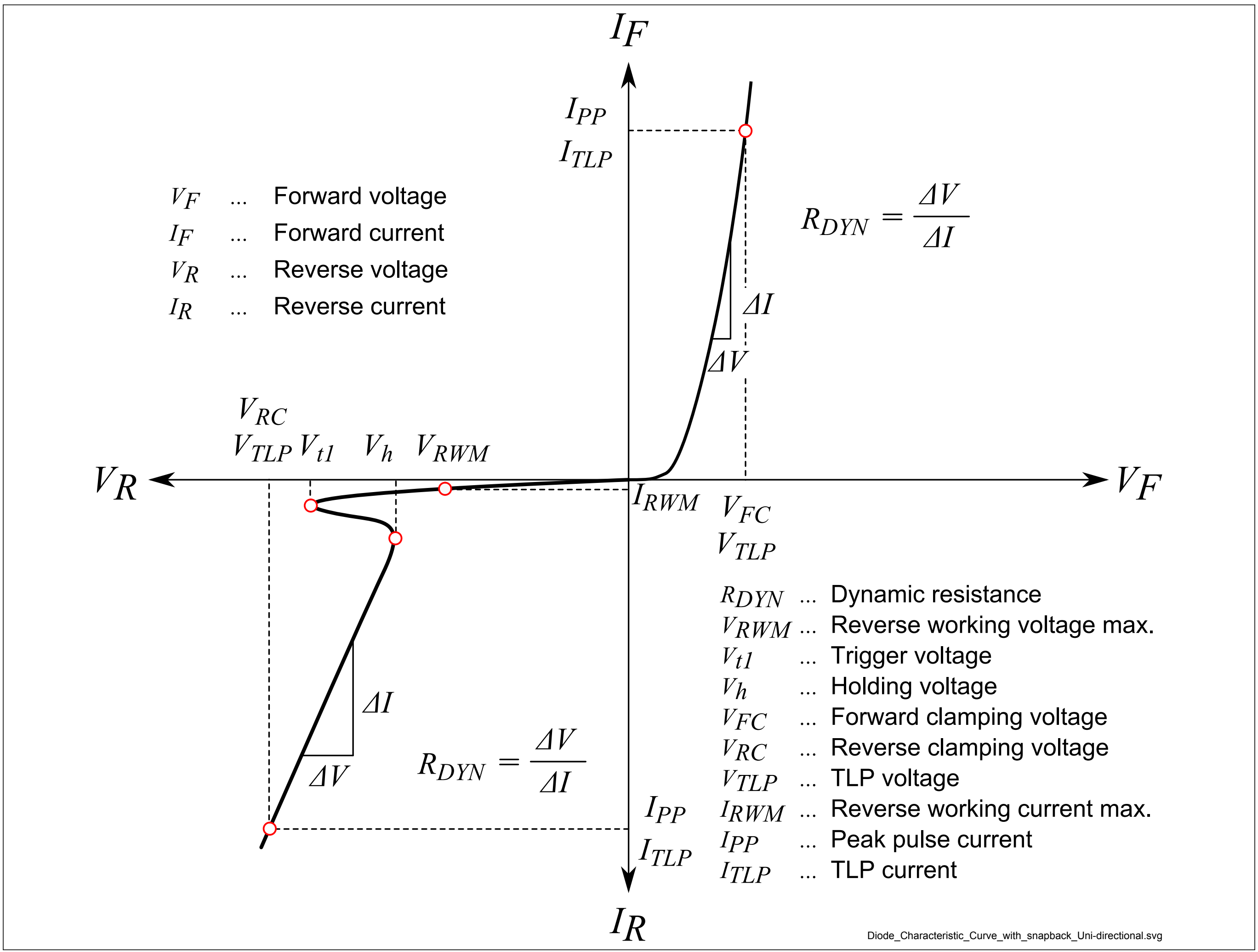

Figure 2 Definitions of electrical characteristics

Table 3 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	3.3	V	–
Reverse current	I_R	–	–	50	nA	$V_R = 3.3$ V

Table 4 RF characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	2	3	pF	I/O to GND, $V_R = 0$ V, $f = 1$ MHz
		–	1	–		I/O to I/O, $V_R = 0$ V, $f = 1$ MHz

Table 5 ESD characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Reverse clamping voltage [1]	V_{CL}	–	4.2	–	V	I/O to GND, $t_p = 8/20$ µs, $I_{PP} = 1$ A
		–	4.9	–		I/O to GND, $t_p = 8/20$ µs, $I_{PP} = 5$ A
		–	5.8	–		I/O to GND, $t_p = 8/20$ µs, $I_{PP} = 10$ A
		–	6.7	–		I/O to GND, $t_p = 8/20$ µs, $I_{PP} = 15$ A
		–	7.7	–		I/O to GND, $t_p = 8/20$ µs, $I_{PP} = 20$ A
Reverse clamping voltage [2]		–	5.8	–		I/O to GND, $t_p = 100$ ns, $I_{PP} = 16$ A
Forward clamping voltage [1]	V_{FC}	–	1.1	–		GND to I/O, $t_p = 8/20$ µs, $I_{PP} = 1$ A
		–	4	–		GND to I/O, $t_p = 8/20$ µs, $I_{PP} = 20$ A
Forward clamping voltage [2]		–	3.1	–		GND to I/O, $t_p = 100$ ns, $I_{PP} = 16$ A
Dynamic resistance [1]	R_{DYN}	–	0.15	–	Ω	I/O to GND, $t_p = 8/20$ µs
Dynamic resistance [2]		–	0.09	–		I/O to GND, $t_p = 100$ ns

1 I_{PP} according to IEC61000-4-5
2 Please refer to application note AN210 [1], TLP parameters: $Z_0 = 50\ \Omega$, $t_p = 100$ ns, $t_r = 300$ ps, averaging window: $t_1 = 30$ ns to $t_2 = 60$ ns, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 10$ A and $I_{PP2} = 40$ A

3 Typical characteristic diagrams

Note: *T_A = 25 °C, unless otherwise specified.*

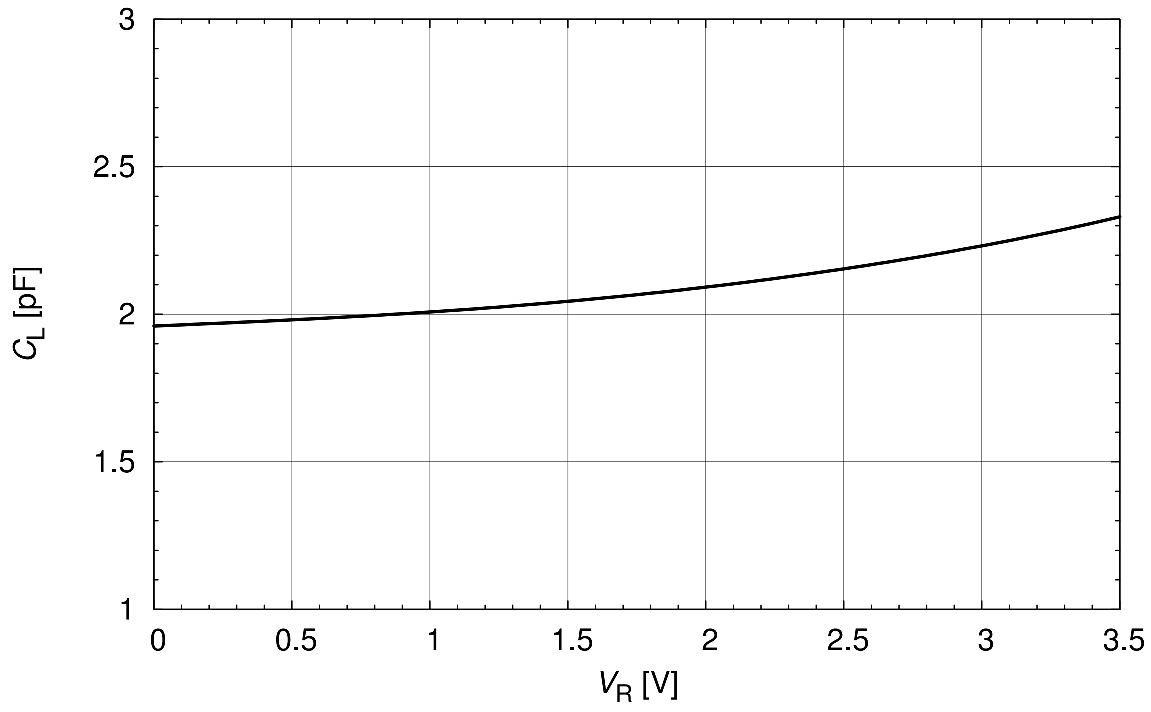

Figure 3 Line capacitance: $C_L = f(V_R)$

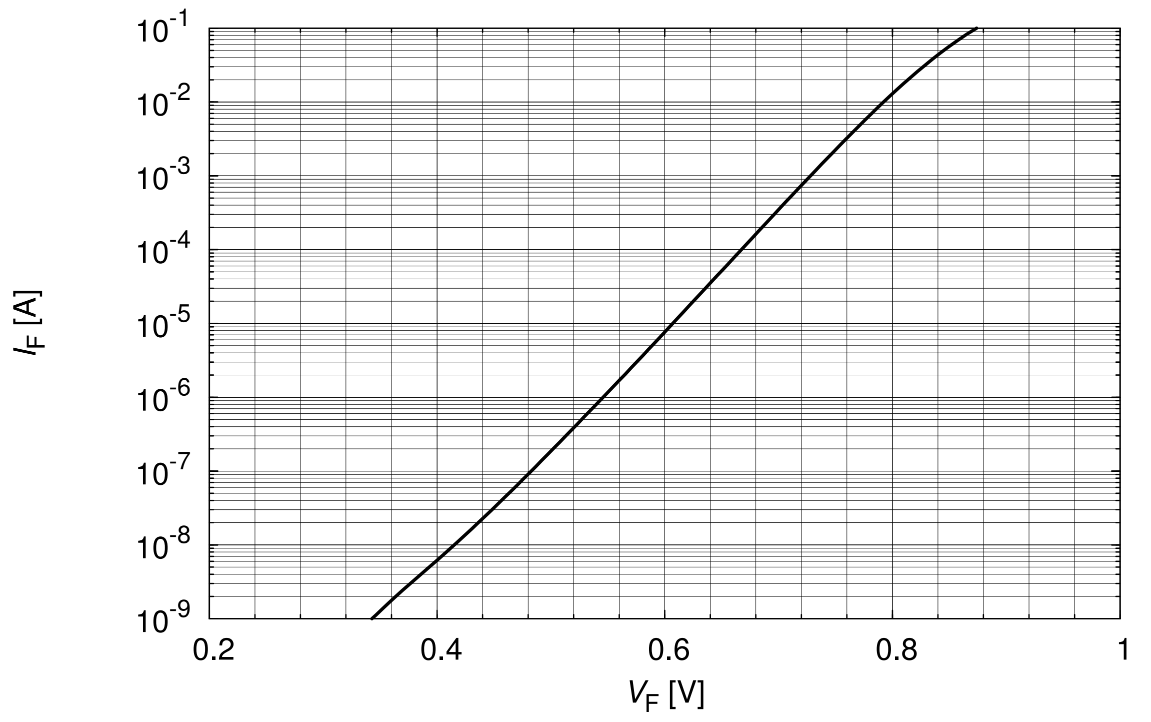

Figure 4 Forward characteristic: $I_F = f(V_F)$

Typical characteristic diagrams

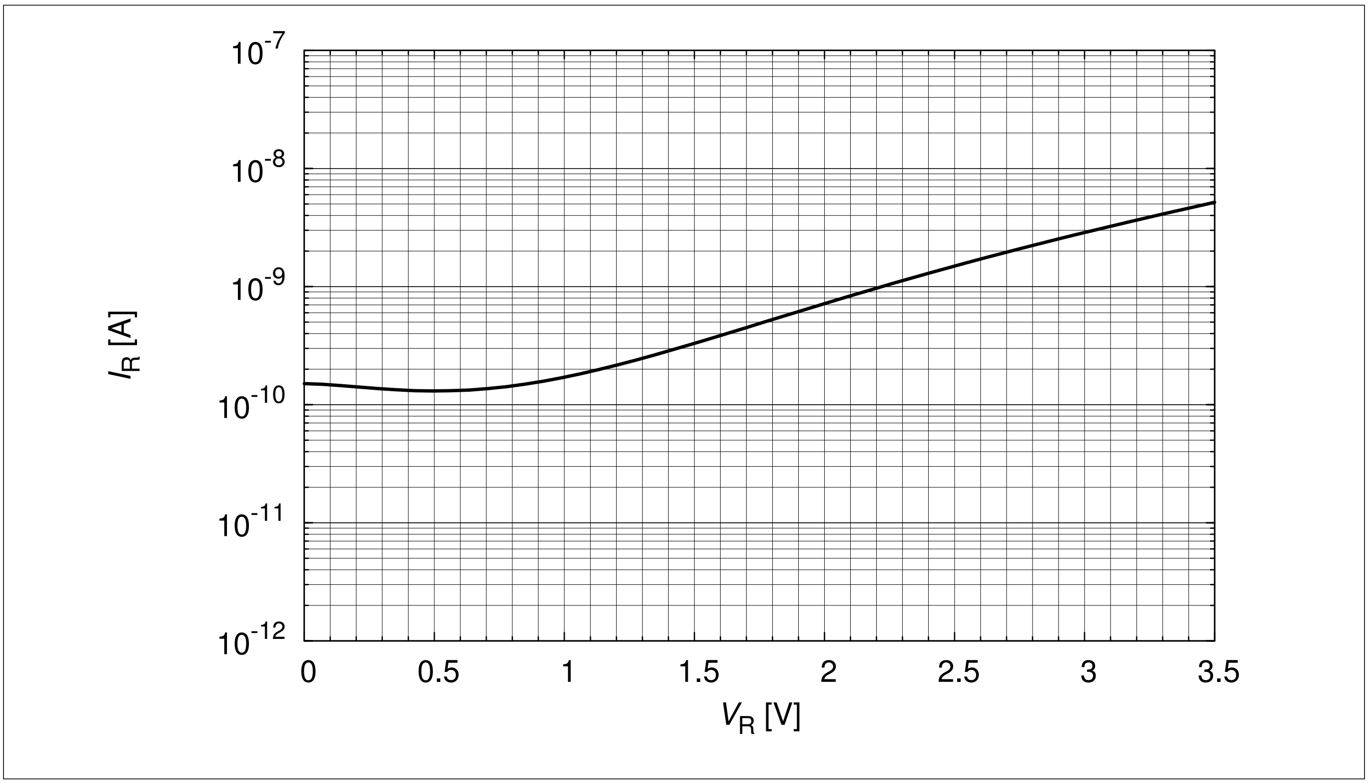

Figure 5 Reverse current: $I_R = f(V_R)$

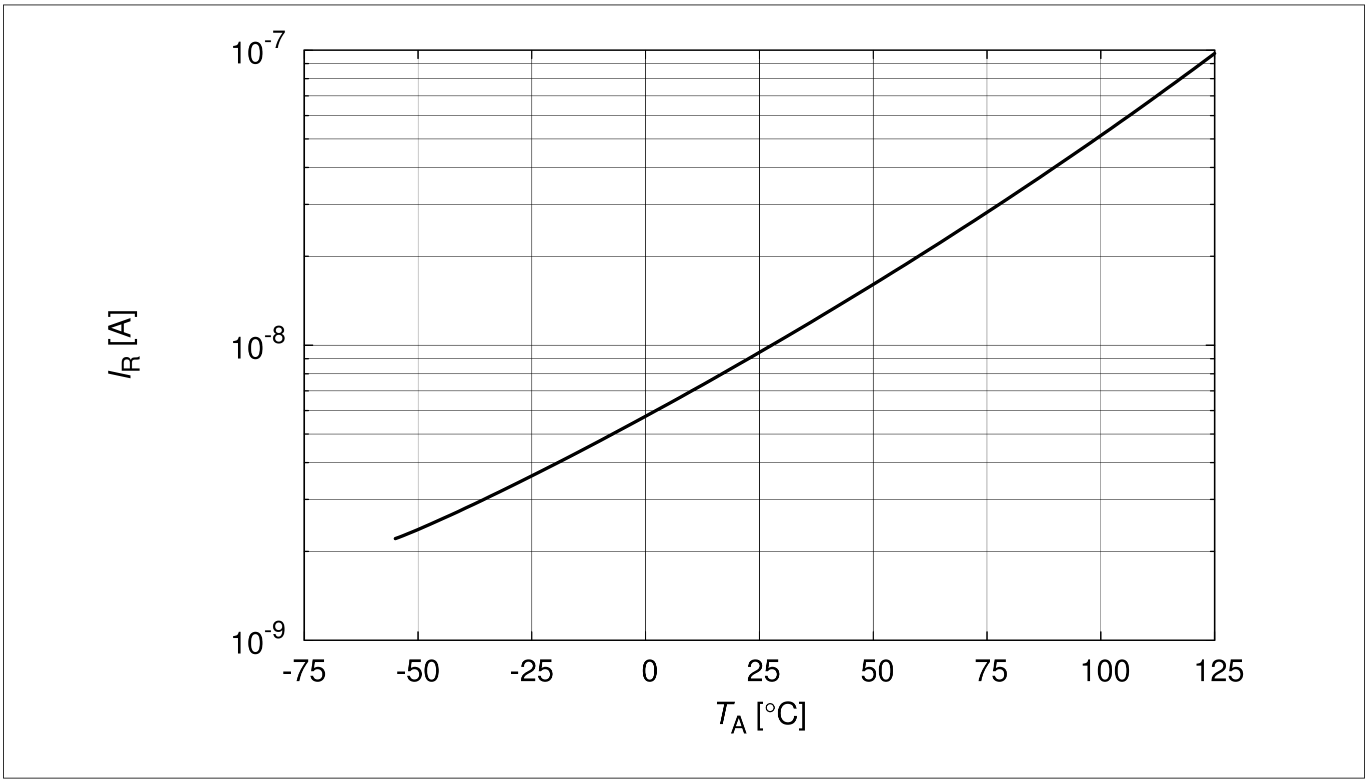

Figure 6 Reverse current: $I_R = f(T_A)$, V_R = 3.3 V

Typical characteristic diagrams

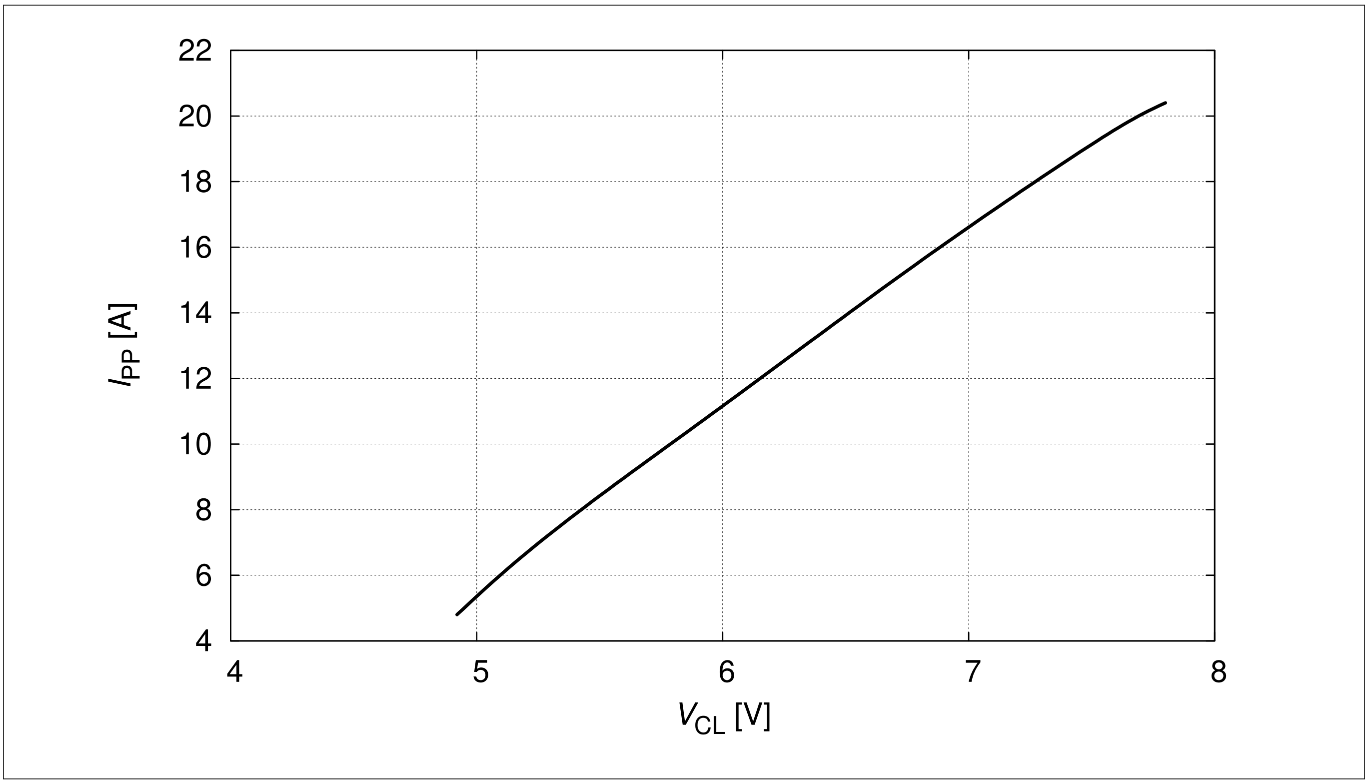

Figure 7 Pulse reverse current versus clamping voltage: I_{PP}= $f(V_{CL})$, according to IEC61000-4-5

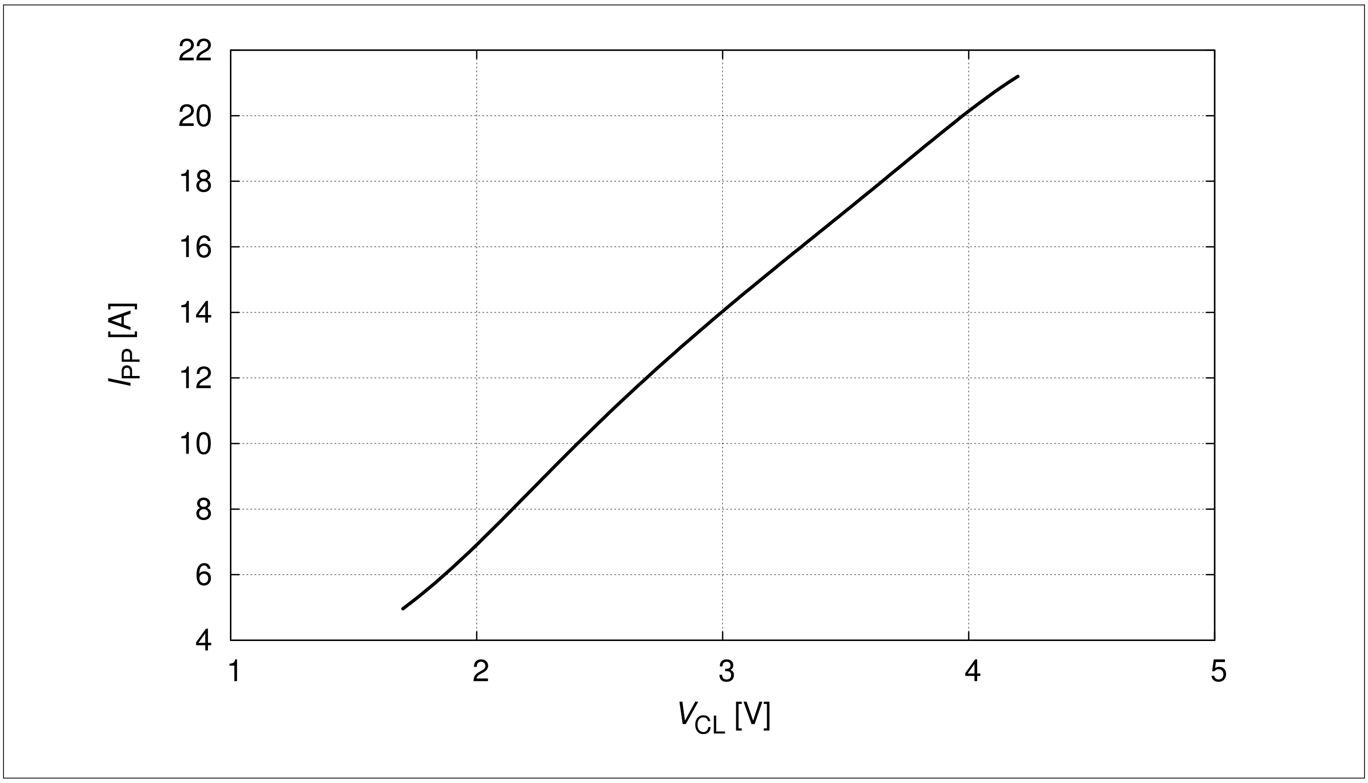

Figure 8 Pulse forward current versus clamping voltage: I_{PP}= $f(V_{CL})$, according to IEC61000-4-5

Typical characteristic diagrams

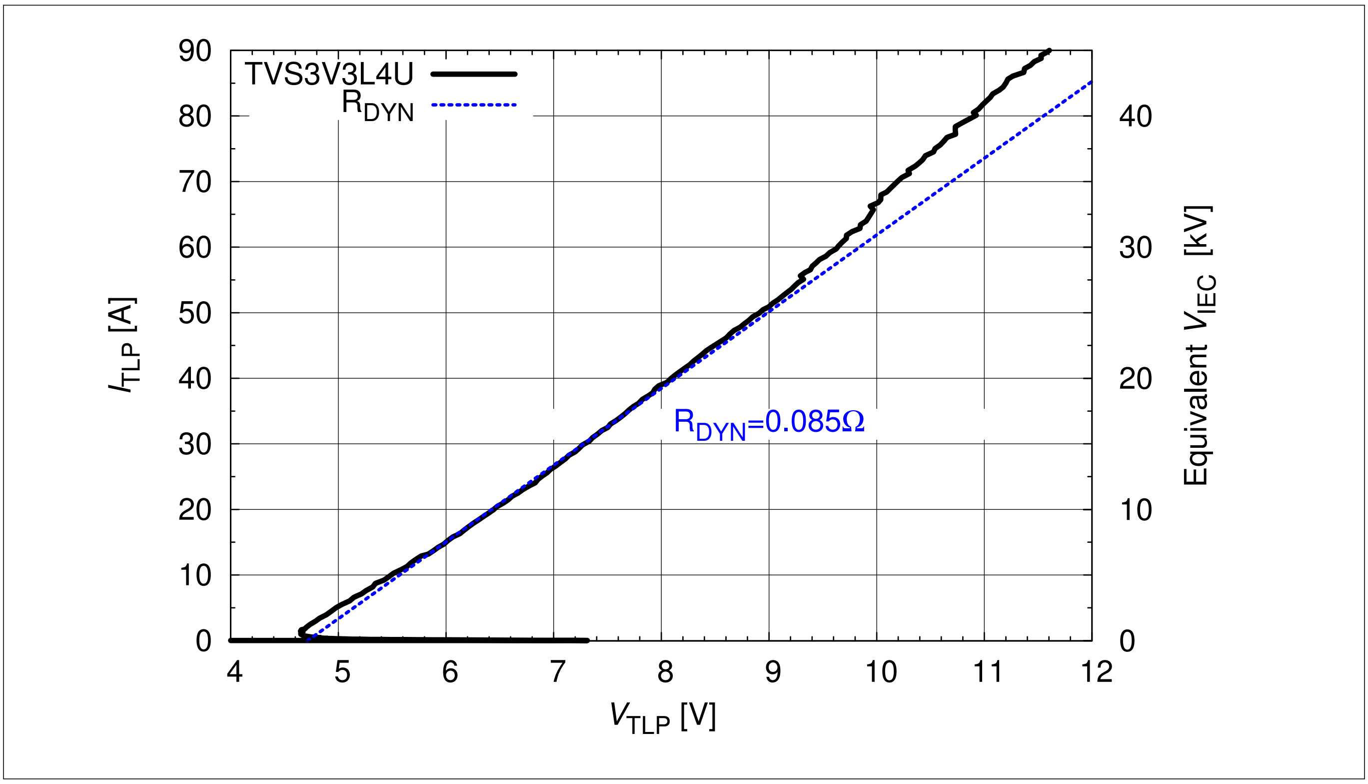

Figure 9 Clamping voltage (TLP): I_{TLP} = f(V_{TLP}), reverse pulse *[1]*

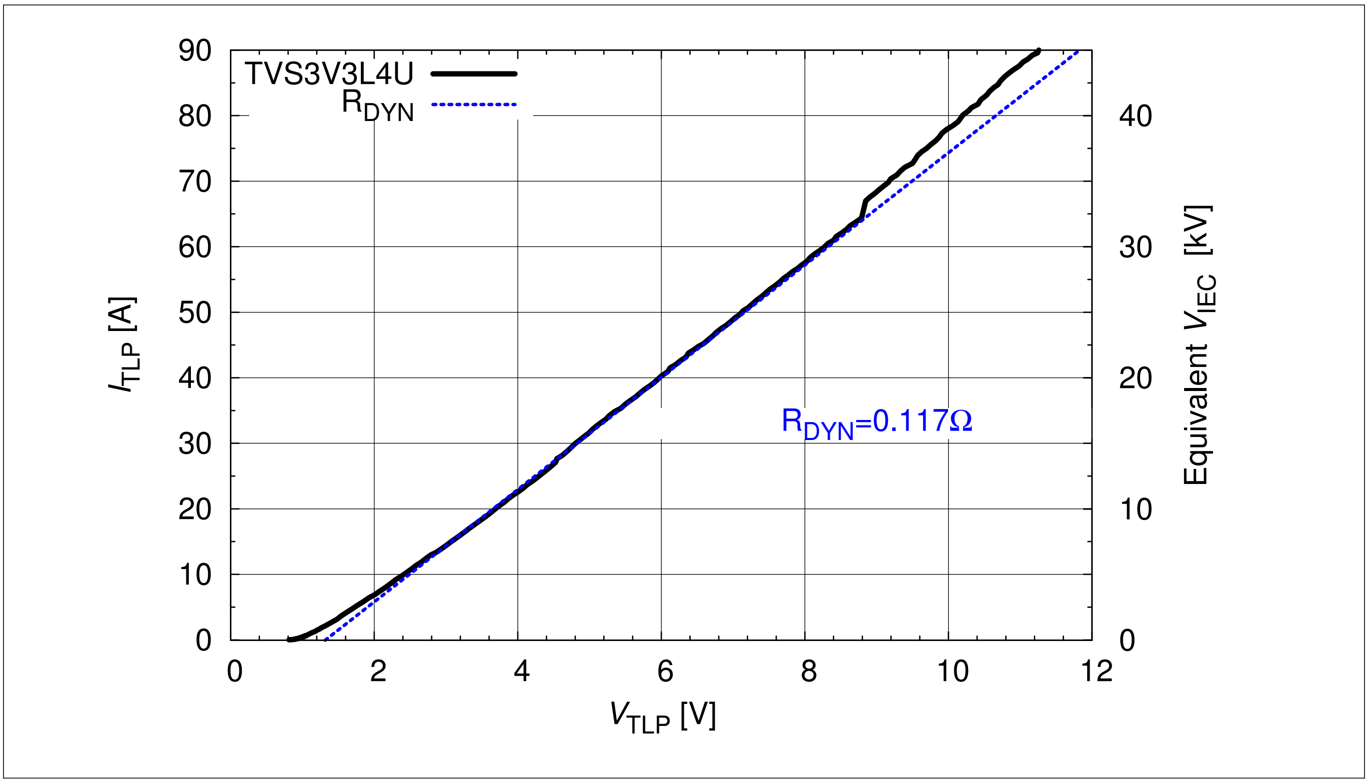

Figure 10 Clamping voltage (TLP): I_{TLP} = f(V_{TLP}), forward pulse *[1]*

Typical characteristic diagrams

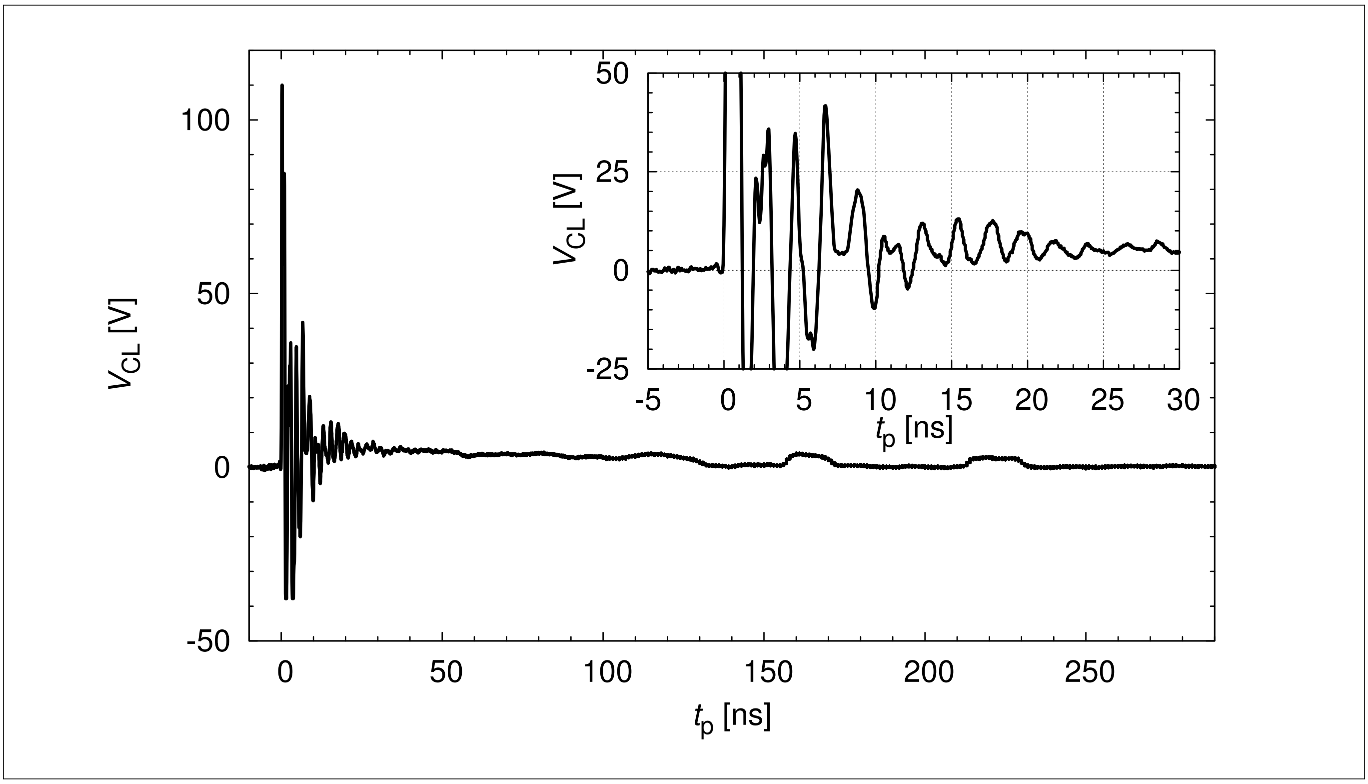

Figure 11 Clamping voltage (ESD): V_{CL} = f(t), 8 kV positive pulse according to IEC61000-4-2

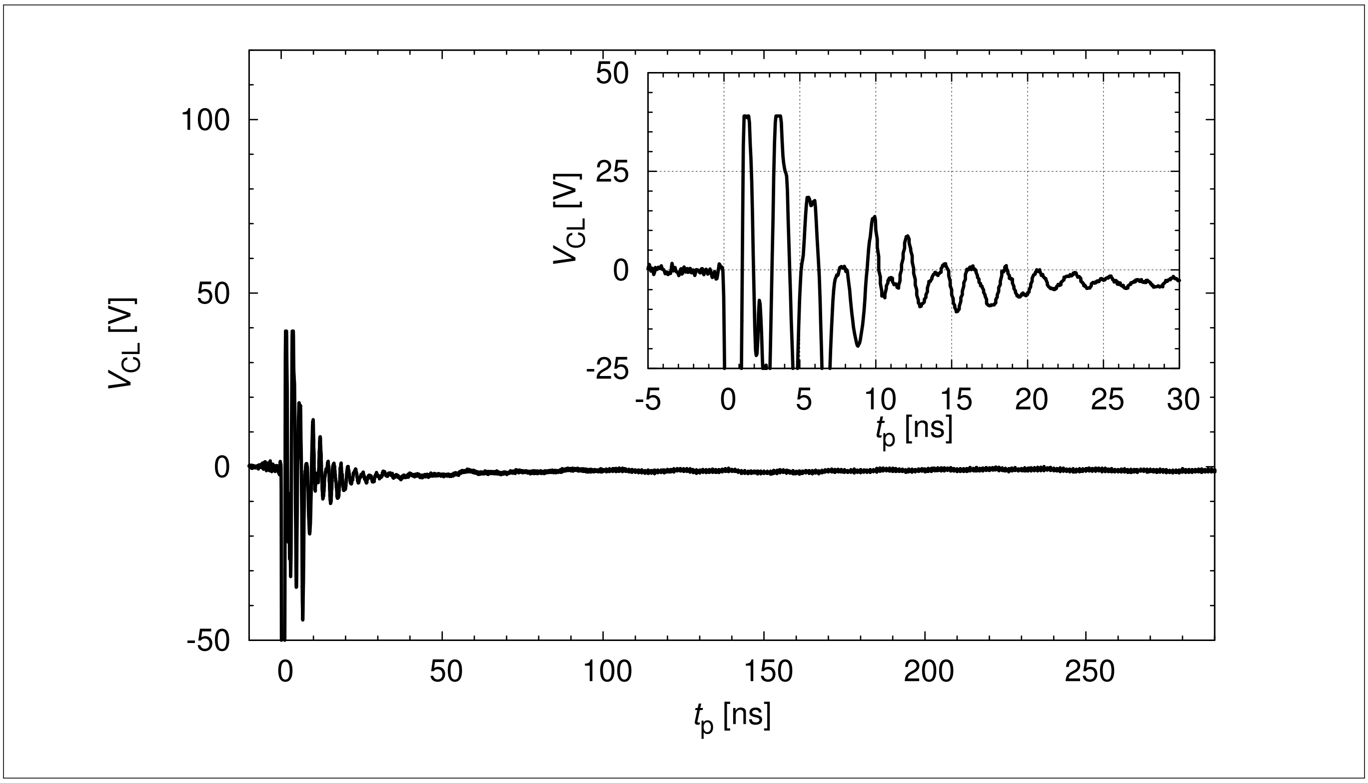

Figure 12 Clamping voltage (ESD): V_{CL} = f(t), -8 kV negative pulse according to IEC61000-4-2

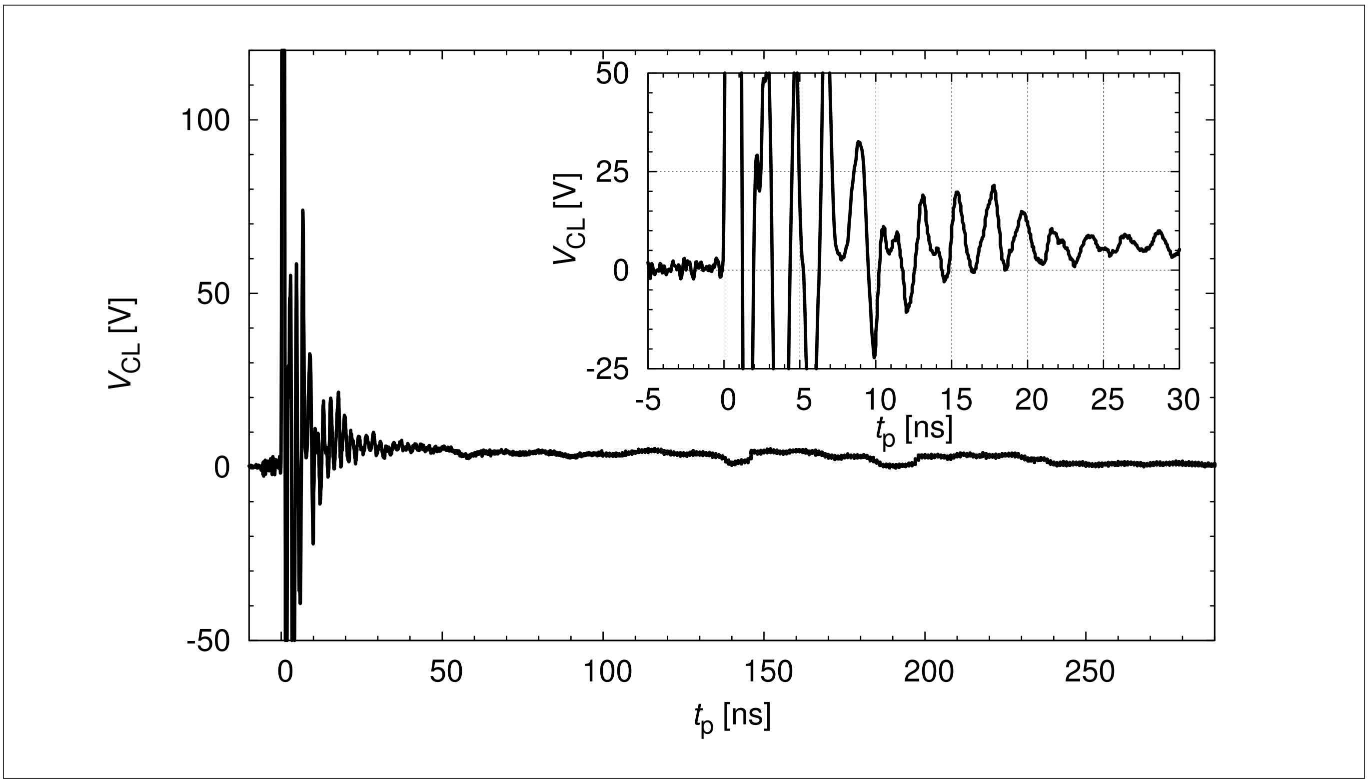

Figure 13 Clamping voltage (ESD): V_{CL} = f(t), +15 kV positive pulse according to IEC61000-4-2

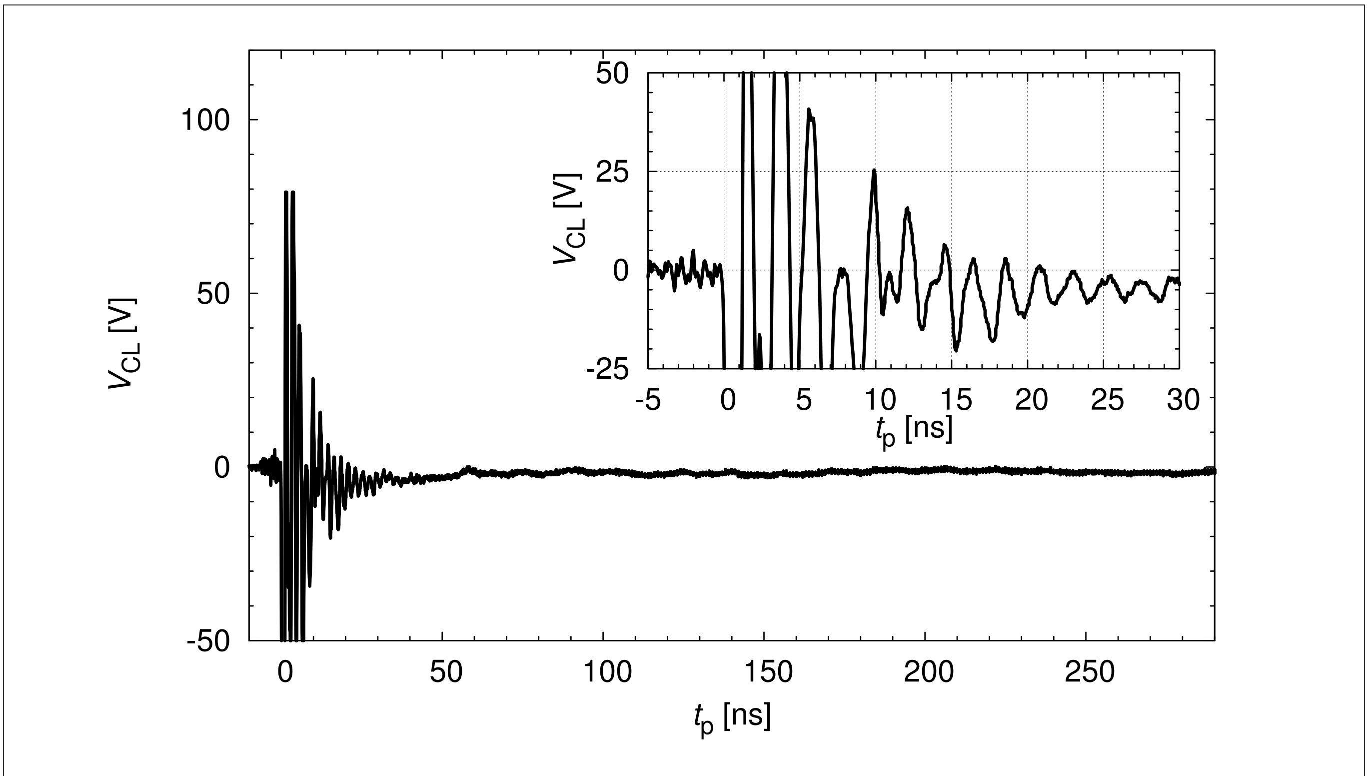

Figure 14 Clamping voltage (ESD): V_{CL} = f(t), -15 kV negative pulse according to IEC61000-4-2

4 Package information

Note: *Dimensions in mm.*

4.1 SC74-6-2 package

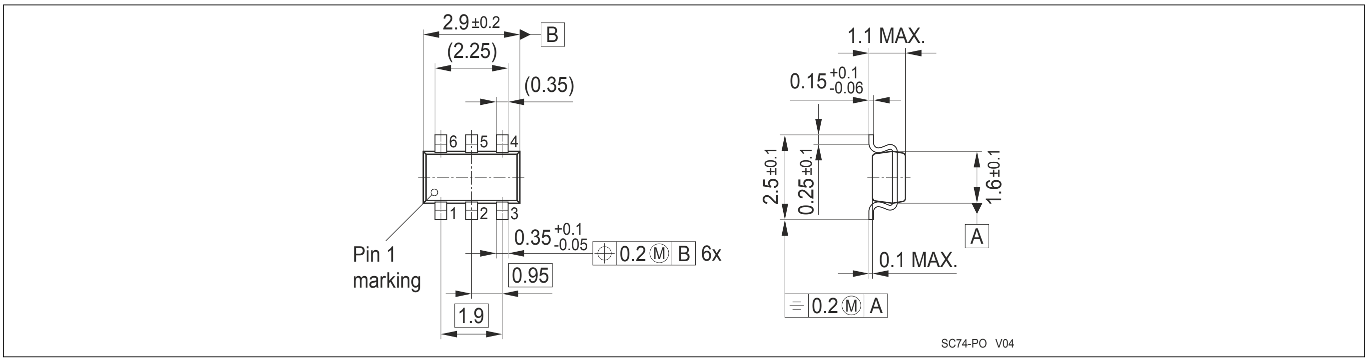

Figure 15 SC74-6-2 package outline

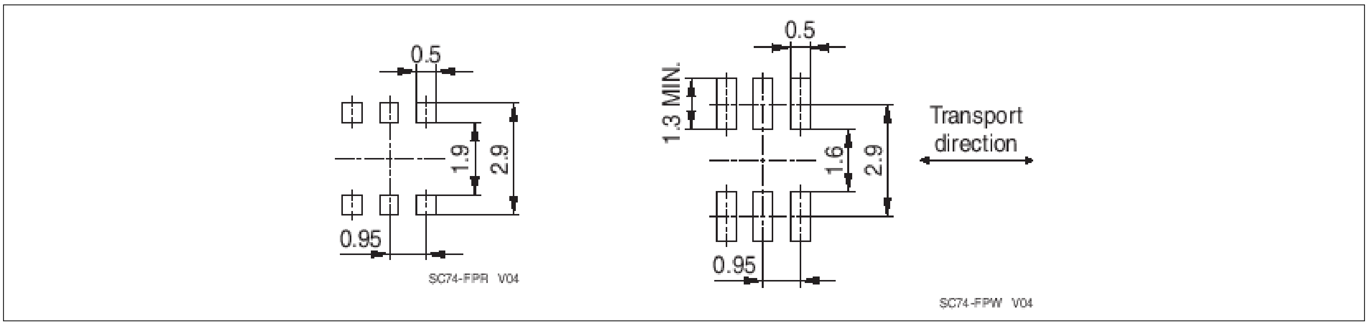

Figure 16 SC74-6-2 footprint

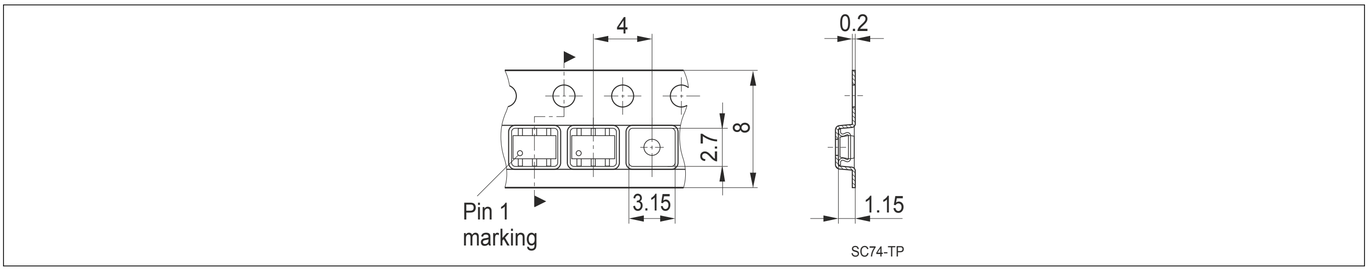

Figure 17 SC74-6-2 packing

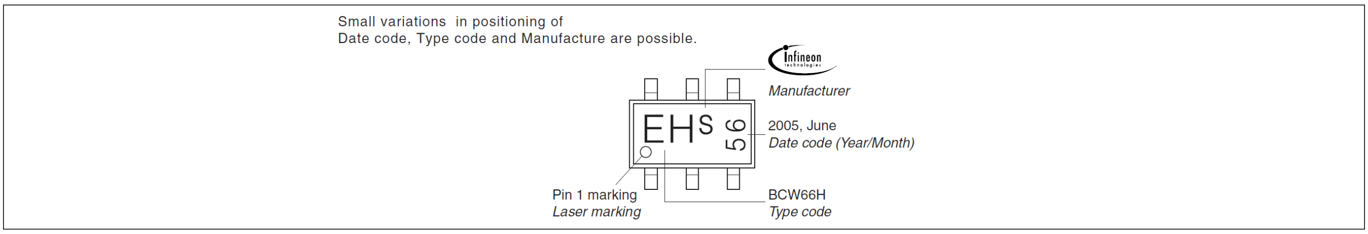

Figure 18 SC74-6-2 marking example (marking code see *Device information*)

5 References

[1] Infineon AG - **Application Note AN210**: Effective ESD protection design at system level using VF-TLP characterization methodology

Revision history

Revision history: Rev. 2.4. 2013-02-06	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.5, 2018-02-16	
All	Data sheet layout changed, editorial changes, references updated

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